What is claimed is:

1. A detector circuit comprising:

an input terminal;

a ground terminal;

an output terminal;

a first device coupled to the input and output terminals, to pull the output terminal to a first output voltage when a supply voltage below a supply threshold is applied to the input terminal, and the first device being configured to have no substantial change in current consumption after the supply voltage applied to the input terminal has exceeded the supply threshold; and

a second device coupled to the input, ground and output terminals, to pull the output terminal to a second output voltage when the supply voltage applied to the input terminal exceeds the supply threshold.

2. The detector circuit of claim 1,wherein the first output voltage is the below supply threshold supply voltage.

3. The detector circuit of claim 1, wherein the second output voltage is ground.

4. The detector circuit of claim 1, wherein the first device is designed with a first operational threshold voltage and the second device is designed with a second operational threshold voltage that is greater the first operational threshold voltage.

5. The detector circuit of claim 1, wherein the first device comprises a depletion transistor device.

6. The detector circuit of claim 1, wherein the first device comprises a depletion NMOS device.

7. The detector circuit of claim 1, wherein

the first device comprises a depletion NMOS device with a drain of the depletion NMOS device coupled to the input terminal, and a source of the depletion NMOS device coupled to a gate of the depletion NMOS device and the output terminal; and

the second device comprises a NMOS device with a drain of the NMOS device coupled to the output terminal, a gate of the NMOS device coupled to the input terminal, and a source of the NMOS device coupled to the ground terminal.

8. A method comprising:

pulling an output terminal, employing a first device, to a first output voltage when a supply voltage below a supply threshold is applied to an input terminal, with the first device configured to have no substantial change in current consumption after the supply voltage applied to the input terminal has exceeded the supply threshold; and

pulling the output terminal, employing a second device, to a second output voltage when the supply voltage applied to the input terminal exceeds the supply threshold.

9. The method of claim 8, wherein the first output voltage is the below supply threshold supply voltage, and the second output voltage is ground.

10. The method of claim 8, wherein the first device is designed with a first operational threshold voltage and the second device is designed with a second operational threshold voltage that is greater the first operational threshold voltage.

11. The method of claim 8, wherein the first device is a depletion NMOS device with a gate of the depletion NMOS device coupled to a source of the depletion NMOS device.

12. A circuit comprising

an input terminal;

a ground terminal;

an output terminal;

a detector circuit having a first plurality of devices, coupled to the input terminal and the ground terminal, to output a first detection voltage when a supply voltage applied to the input terminal is below a supply threshold, and a second detection voltage when the supply voltage exceeds the supply threshold, with at least one of the first plurality of devices configured to have no substantial change in current consumption after the supply voltage has exceeded the supply threshold; and

a switching circuit coupled to the input, ground and output terminals, and to the detector circuit, to couple the output terminal to ground when the detector circuit outputs the first detection voltage, and couple the supply voltage to the output terminal when the detector circuit outputs the second detection voltage.

13. The circuit of claim 12,wherein the first detection voltage is the below supply threshold supply voltage, and the second detection voltage is ground.

14. The circuit of claim 12, wherein the detector circuit comprises a first device designed with a first operational threshold voltage and a second device designed with a second operational threshold voltage that is greater the first operational threshold voltage.

15. The circuit of claim 12, wherein the detector circuit comprises

a depletion NMOS device with a drain of the depletion NMOS device coupled to the input terminal, and a source of the depletion NMOS device coupled to a gate of the depletion NMOS device and the switching circuit; and

a NMOS device with a drain of the NMOS device coupled to the switching circuit, a gate of the NMOS device coupled to the input terminal, and a source of the NMOS device coupled to the ground terminal.

16. The circuit of claim 12, wherein the switching circuit comprises

a PMOS device with a source of the PMOS device coupled to the input terminal, a drain of the PMOS device coupled to the output terminal, and a gate of the PMOS device coupled to the detector circuit; and

a NMOS device with a drain of the NMOS device coupled to the output terminal, a gate of the NMOS device coupled to the detector circuit, and a source of the NMOS device coupled to the ground terminal.

17. A method comprising:

pulling an output terminal to ground with a switching circuit responding to a first detection voltage outputted by a detector circuit when a supply voltage is below a supply threshold, the detector circuit including a plurality of devices, where at least a first of the plurality of devices is configured to consume substantially a same amount of current when the supply voltage is below the supply threshold, and when the supply voltage exceeds the supply threshold; and

pulling the output terminal to the supply voltage, with the same switching responding to a second detection voltage outputted by the detector circuit when the supply voltage exceeds the supply threshold.

18. The method of claim 17,wherein the first detection voltage is the below supply threshold supply voltage, and the second detection voltage is ground.

19. The method of claim 17, wherein the first device of the detector circuit is designed with a first operational threshold voltage, and the detector circuit further comprises a second device designed with a second operational threshold voltage that is greater the first operational threshold voltage.

20. The method of claim 17, wherein the first device of the detector circuit is a depletion NMOS device with a gate of the depletion NMOS device coupled to a source of the depletion NMOS device.

21. A system, comprising:

a component having a detector circuit to detect application of a supply voltage applied to the component, the detector circuit including a plurality of devices, where at least one of the devices is configured to consume substantially a same amount of current when the supply voltage is below a supply threshold and when the supply voltage is above the supply threshold; and

a bus coupled to the component;

a communication interface coupled to the bus to facilitate communication with another system.

22. The system of claim 21, wherein the detector circuit is designed to output the supply voltage when the supply voltage is below the supply threshold, and ground its output when the supply voltage exceeds the supply threshold.

23. The system of claim 21, wherein the first device of the detector circuit is designed with a first operational threshold voltage, and the detector circuit further comprises a second device designed with a second operational threshold voltage that is greater the first operational threshold voltage.

24. The system of claim 21, wherein the first device of the detector circuit is a depletion NMOS device with a gate of the depletion NMOS device coupled to a source of the depletion NMOS device.

25. The system of claim 21, wherein the component further comprises a switching circuit coupled to the detector circuit, to output the supply voltage when the supply voltage exceeds the supply threshold, and ground its output when the supply voltage is below the supply threshold.

26. The system of claim 25, wherein the switching circuit comprises

a PMOS device with a source of the PMOS device coupled to receive the supply voltage, a drain of the PMOS device coupled to an output terminal of the switching

circuit to output the supply voltage or be grounded, and a gate of the PMOS device coupled to the detector circuit; and

a NMOS device with a drain of the NMOS device coupled to the output terminal of the switching circuit, a gate of the NMOS device coupled to the detector circuit, and a source of the NMOS device coupled to ground.

27. The system of claim 21, wherein the component is a selected one of a microprocessor and a chipset.

28. The system of claim 21, wherein the system is a selected one of a wireless mobile phone, a personal digital assistant, a set-top box, a CD player, a DVD player, and a digital camera.